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STUDY AND ANALYSIS OF CHARGE PUMP CIRCUITS AND INDUCTOR BASED DC-DC CONVERTERS FOR MOBILE APPLICATIONS

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Abstract

The mobiles market is very active; constructors do not stop to add functionalities to their mobiles. Power supplies relies on batteries .However batteries provide a limited operating time and ustable voltage ; given the highly variable nature of batteries (e.g., 2.7–4.2 V for Li-ion), systems often require supply voltages to be both higher and lower than the battery voltage (e.g., power amplifier for CDMA applications).In order to ensure a correct behavior of embedded sub-circuits of mobiles which need a stable and clean voltage , DC-DC converters are employed to generate different stable and fixed voltage from battery.

Keywords:

Portable applications ;
Inductor DC-DC converters ;
Charge pumps ;
Regulation mode.

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1. Introduction

Mobiles devices have become inseparable parts of people's lives in recent times. The demand for thin, lightweight and multifunctional mobiles is growing day-to-day. Mobiles are powered from single battery and they should be able to operate for an extended period of time. They have a large number of circuit sub-systems which require different voltage domains to operate. In this context , DC-DC converters are used to generate secondary constant voltage from battery ; they are used to step up or step down the input power supply. DC-DC converters are electronic circuits that change the DC operating voltage or current. They have a particular interest in low-powercircuits, as cellular phone. This sort of technology are composed of many sub-circuits that require an own voltage level from an external supply (higher, lower or even negative) or battery.

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DC-DC converters have a special role in these kind of systems, since they can be employed to change the voltage from a partial lowered battery voltage thereby. Fig.1 shows the block diagram of a general DC/DC regulator which contains two main blocks; power processor and feedback control part. The feedback control part senses the output voltage and adjusts the power transfer by generating corrective control signals to keep the output voltage constant[1].

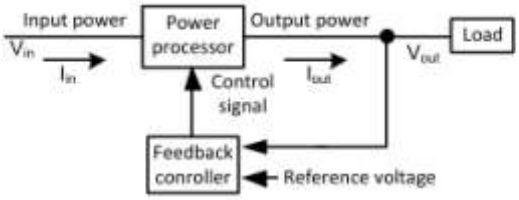

Figure 1. *Block diagram of DC/DC converter*

2. Inductor based DC/DC converters

Inductor-based DC-DC converters architecture has dominated moderate and high-power integrated circuit applications. They generally uses an inductor, a switch, a diode and a load capacitor which is used to store the energy required to be delivered to the load [2]. Different topologies of DC-DC converter (i.e., buck converter, boost converter, inverting converter) can be derived by placing the inductor in different ways in the circuit. In the following approaches, converters are supposed to operate in steady-state with a constant input voltage and a constant output voltage. Further, the components are taken ideal and no parasitics are considered (e.g, the power transistors are assimilated to ideal switches having an infinite resistance when turned off, and no resistance when turned on). The main topologies of inductor based DC/DC converters are shown in Fig.2 [3].

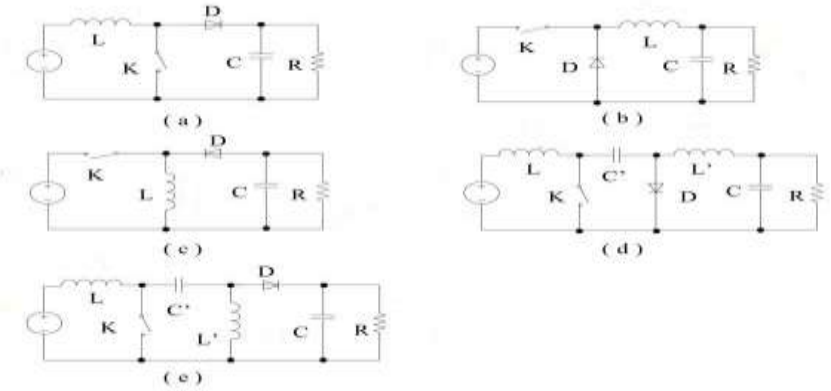

Figure 2. *(a) Boost converter, (b) Buck converter,(c)Buck-Boost converter, (d)Cuck converter,(e) Sepic converter*

2.1. Buck converter

The buck converter is a commonly used in circuits that steps down the voltage level from the input voltage according to the requirement. It has the advantages of simplicity and low cost. When the switch is open , no current flow through any part of circuit. When the switch is closed, the current flows through the inductor, slowly at first, but building up over time. When the switch is closed the inductor pulls current through the diode, and this means the voltage at the inductors "output" is lower than it first was. This is the very basic principle of operation of buck circuit [4].

It can operate in Condinous conduction mode (CCM) and Discontinuous Conduction Mode (DCM).

In CCM, the inductor current never falls to zero during the commutation cycle.
During (ON state) ; the switch is closed , the voltage across inductor is given by:

$$V_L = V_{IN} - V_{OUT} \quad (1)$$

During (OFF state) ; the switch is open and diode is reverse-biased , voltage across the inductor is

$$V_L = -V_{OUT} \quad (2)$$

The increase of current during ON state is given by :

$$\Delta I_{LON} = \int_0^{t_{ON}} \frac{V_L}{L} dt = \frac{V_{IN} - V_{OUT}}{L} t_{ON} \quad (3)$$

The decrease of current during OFF state is given by :

$$\Delta I_{LOFF} = \int_{t_{ON}}^{t_{OFF}} \frac{V_L}{L} dt = \frac{-V_{OUT}}{L} t_{OFF} \quad (4)$$

In steady state :

$$\frac{V_{IN} - V_{OUT}}{L} t_{ON} - \frac{V_{OUT}}{L} t_{OFF} = 0 \quad (5)$$

Where $t_{ON} = DT$, $t_{OFF} = (1-D)T$, D represents the duty cycle as shown in Fig3.

As a result :

$$D = \frac{V_{OUT}}{V_{IN}} \quad (6)$$

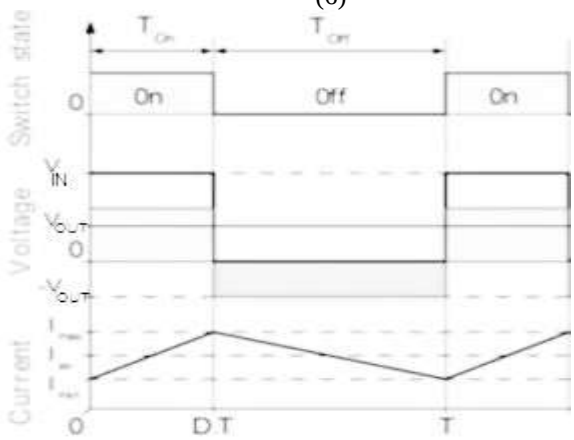

Figure 3. *Evolution of voltage and current of a buck converter in CCM*

In Discontinuous Conduction Mode (DCM) , current through the inductor falls to zero during a part of the period , the amount of energy required by the load is small enough to be transferred in a time lower than the whole commutation period as shown in Fig 4.

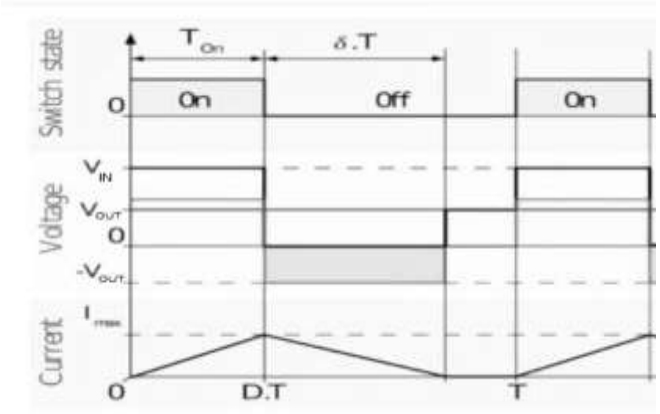

Figure 4. *Evolution of voltage and current of a buck converter in DCM*

The converter operates in steady state , the energy of the inductor is the same at the beginning and at the end of the cycle .Previous equations will be written as:

$(V_{IN} - V_{OUT})DT - V_{OUT} * \delta T = 0$ As a consequence , we obtain :

$$\delta = \frac{V_{IN} - V_{OUT}}{V_{OUT}} D \quad (6)$$

The output capacitor is large enough to maintain a constant voltage across its terminals during a commutation cycle. This implies that the current flowing through the capacitor has a average value ,So:

$$< I_L >= (\frac{1}{2} I_{LMax} DT + \frac{1}{2} I_{LMax} \delta T) \frac{1}{T} = \frac{I_{LMax}(D+\delta)}{2} = I_{OUT} \quad (7)$$

The inductor current is zero at the beginning and rises during ON time up to its maximum value so

$$I_{LMax} = \frac{V_{IN} - V_{OUT}}{L} DT \quad (8)$$

Substituting the value of I_{LMax} in the previous equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT})DT(D+\delta)}{2L} \quad (9)$$

And substituting δ by its expression, we obtain:

$$V_{OUT} = V_{IN} \frac{1}{\frac{2LI_{OUT}}{D^2 V_{IN} T} + 1} \quad (10)$$

The output voltage of a buck converter operating in DCM in afunction of input voltage , duty cycle ,inductor value commutation period and output current .

2.2. Boost Converter

Boost converter is one of the simplest but most useful power converters. It is a step-up converter that converts an unregulated DC input voltage to a regulated dc output at a lower voltage [5]. Boost converters start their voltage conversion with a current flowing through the inductor (switch is closed). Then they close the switch leaving the current no other path to go than through a diode (functions as one way valve) The current then wants to slow really fast and

the only way it can do this is by increasing it's voltage (akin to pressure) at the end that connects to the diode, and switch. If the voltage is high enough it opens the diode, and one through the diode, the current can't flow back. This is the very basic concept of boost converter[4].

Like buck converter , boost can operate in Continuous Conduction Mode and Discontinuous Conduction Mode

In Continuous Conduction Mode (CCM) we obtain :

$$V_{OUT} = V_{IN} \frac{1}{1-D}$$

In Discontinuous Conduction Mode (DCM) we obtain :

$$V_{OUT} = V_{IN}(1+\frac{V_{IN}D^2T}{2LI_{OUT}}) \quad (12)$$

2.3. Buck- Boost Converter

Buck-Boost converter can deliver an output voltage higher or lower than the input voltage.

In Continuous Conduction Mode (CCM) , during ON state , switch is closed , the increase of inductor current is given by :

$$\Delta I_{LON} = \int_0^{DT} dI_L = \int_0^{DT} \frac{V_L}{L} dt = \frac{V_{IN}DT}{L} \quad (13)$$

Durin OFF state, the switch is open and the inductor current flows through the load. The variation of inductor current is given by :

$$\Delta I_{LOFF} = \int_0^{(1-D)T} dI_L = \int_0^{(1-D)T} \frac{V_{OUT}}{L} dt = \frac{V_{OUT}(1-D)T}{L} \quad (14)$$

In steady state conditions $\Delta I_{LON} = \Delta I_{LOFF}$

This expression yields :

$$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D} \quad (15)$$

As the duty cycle D goes from 0 to 1 , the polarity of the output voltage is negative.

In Discontinuous Conduction Mode , we obtain :

$$\frac{V_{OUT}}{V_{IN}} = \frac{-V_{IN}D^2T}{2LI_{OUT}} \quad (16)$$

2.4. Cuck Converter

The Cuk converter is used for getting the output voltage with different polarity. That means output voltage magnitude can be either larger or smaller than the input, and there is a polarity reversal on the output.The inductor on the input acts as a filter for the dc supply, to prevent large harmonic current. Unlike the previous converter topologies where energy transfer is associated with the inductor. Energy transfer for the cuk converter depends on the capacitor C1[4].

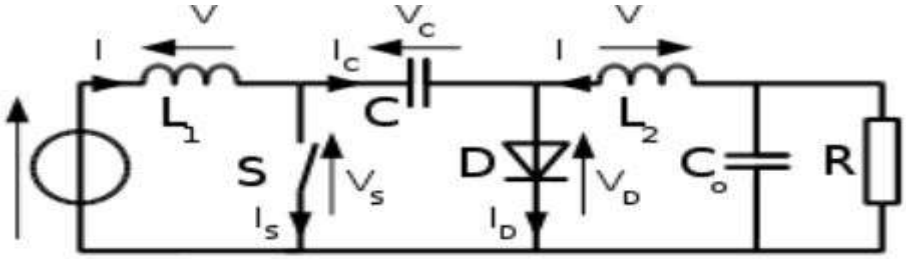

Figure 5. *Cuck converter*

As with other converters (buck converter, boost converter, buck-boost converter), the cuk converter can either operate in continuous or discontinuous current mode. However, unlike these converters, it can also operate in discontinuous voltage mode (i.e., the voltage across the capacitor drops to zero during the commutation cycle).

Supposing the cuck converter operating in Continuous Conduction Mode , in steady state conditions , the energy stored in inductors is the same at the beginning and the end of commutation cycle .The energy in an inductor is given by :

$$E = \frac{1}{2} LI^2$$

So , current through the inductor is the same at the beginning and the end of the commutation cycle

$$V_L = L\frac{dI}{dt}$$

During off state, inductor L_1 is connected in series with V_{IN} and C .So :

$$V_{L1} = V_{IN} - V_C \quad (17)$$

As the diode is forward biased , L_2 is connected to output capacitor .So :

$$V_{L2} = V_{OUT} \quad (18)$$

During ON state , L_1 is directly connected to the input source .So :

$$V_{L1} = V_{IN} \quad (19)$$

Inductor L_2 is connected in series with C and the output capacitor .So :

$$V_{L2} = V_{OUT} + V_C \quad (20)$$

The converter operates in ON state from t=0 to t=DT and in OFF state from DT to T

During a period equal to (1-D)T, the average value of V_{L1} and V_{L2} are :

$$< V_{L1} >= DV_{IN} + (1-D)(V_{IN} - V_C) = (V_{IN} - (1-D)V_C) \quad (21)$$

$$< V_{L2} >= D(V_{OUT} + V_C) + (1-D)(-V_{OUT}) = V_{OUT} + DV_C \quad (22)$$

In steady state conditions, both average voltage have to be zero .So:

$$< V_{L1} >= V_{IN} + (1-D)\frac{V_{OUT}}{D} = 0 \quad (23)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} \quad (24)$$

The relation is the same as that obtained for Buck-Boost converter.

3. Charge pumps converters

A DC–DC charge pump circuit provides a DC voltage that is higher than the DC voltage of the power supply or provides a voltage of a reverse polarity. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load and do not involve amplifiers or transformers.For that reason,a charge pump is a device of choice in semiconductor technology where normal range of operating voltages is limited [6].

3.1. Charge pumps topologies

One of the best-known topologies is the voltage doubler. Fig. 6 shows the basic switch configuration and the necessary capacitors for a voltage doubler charge pump .

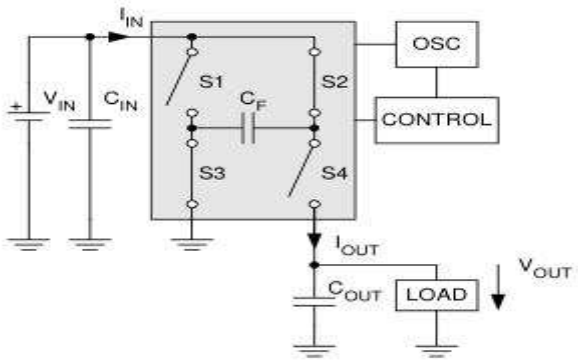

Figure 6. *Voltage doubler charge pump*

The operation of a charge pump can be divided into two phases: In Phase 1, also called charge phase, the switches S2 and S3 are closed and the flying capacitor C_F is ideally charged to V_{IN}. During this time, the output capacitor C_{OUT} supplies the load and is therefore being discharged. In Phase 2, also called transfer phase, the switches S1 and S4 are closed and the flying capacitor C_F is placed in series to the input voltage. These two voltage sources charge the output capacitor C_{OUT} and supply the load. Phases 1 and 2 have a duty cycle of 50%, i.e. both have the same duration, Δt. To transfer energy from the input to the output, the phases are periodically repeated with a frequency of several hundred kiloHertz. A control circuitry and an oscillator control the operation of the charge pump.[7]

Fig.7 depicts four different boost type charge pump architectures which are basic cascaded voltage doubler, ladder, Fibonacci and multi-phase voltage doubler. Each of them has different orientation of the charge transfer switches and capacitors and different charge transfer sequence [8] . Each architecture has a voltage doubler as a basic cell

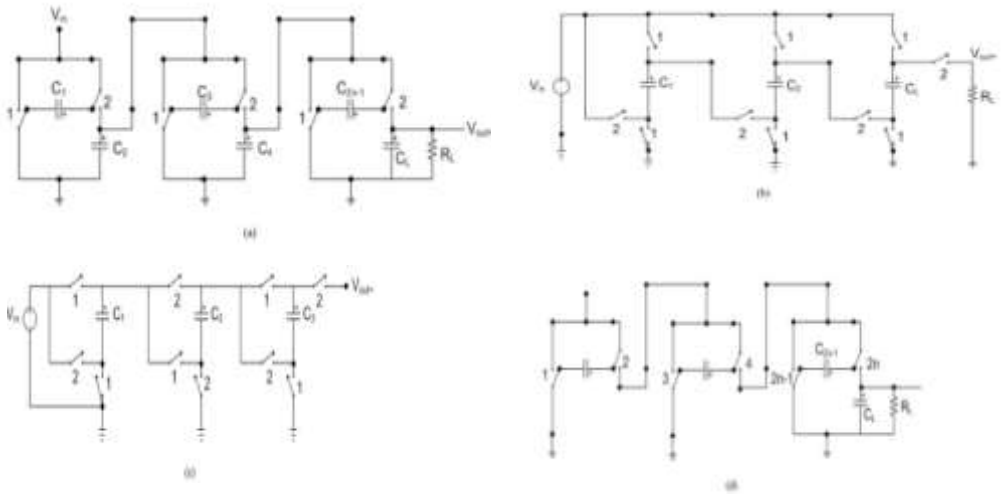

Figure 7: (a) Dual phase cascaded voltage doubler (b)Ladder charge pump (c)Fibonacci charge pump (d)Multiphase cascaded charge pump

Dual phase voltage doubler the charge transfer action in the voltage doubler is controlled by two non-overlapping clocks. The ideal voltage gain for the dual phase voltage doubler with N stages is A = 2*N [10] . In order to perform switching action, an N-stage dual phase voltage doubler involves 4*N charge transfer switches. As the charge pump architecture is designed fully on-chip or partially on-chip with external capacitors, the available silicon area and the number of pins are critical constraints for an analog designer. For the dual phase voltage doubler with N stages, the optimal performance can be achieved by using 2*N capacitors with equal capacitance value [9] .

Ladder charge pump the gain of a ladder with N stages is 2*N , an N-stage ladder charge pump requires 4*N charge transfer switches. To optimize the performance, 2*N capacitors with equal capacitance value are required for the ladder charge pump architecture with N stages.

Fibonacci charge pump architecture During his study of the switched-capacitor voltage multipliers, Makowski developed a new orientation of the switch-capacitor charge pump which has voltage gain related to the Fibonacci numbers [10] . An N-stage Fibonacci charge pump architecture has 3*N+1 charge transfer switches and has gain equal to (N+3) th number of the Fibonacci sequence

Multiphase charge pump architecture An N-stage multiphase charge pump architecture can provide 2 N voltage gain with 4*N charge transfer switches and (2*N+1) capacitors of equal value. However, it requires 2*N clock signals which can be easily generated by a frequency division scheme [9] .

3.2. Regulated charge pumps Vs Unregaleted charge pumps

The topologies shown up to now have been unregulated and deliver a multiple of the input voltage. In most applications, this would lead to the need for an additional regulator to regulate the output voltage if the input voltage varies, as with batteries. To overcome this disadvantage newer charge pumps are regulated and deliver a fixed output voltage. There are actually different ways to regulate a charge pump [7].

Pulse Skip Regulation Method: In the pulse skip control scheme, the output voltage of the charge pump is maintained at the desired value by omitting the unnecessary clock pulses [10]. The regulated charge pump architecture with the pulse skip regulation method and the switching signals are shown in Fig. 8. When the output voltage goes lower than the reference voltage, the output load capacitance is charged continuously during each clock cycle. When the output voltage

is higher than the reference voltage, some clock pulses are skipped and the charge pump stop providing energy to the load. During the pulse skipping, the average input current is quite low, which is advantageous. However, the output ripple voltage in the pulse skip regulation scheme and large frequency variation in the clock signal are disadvantages .

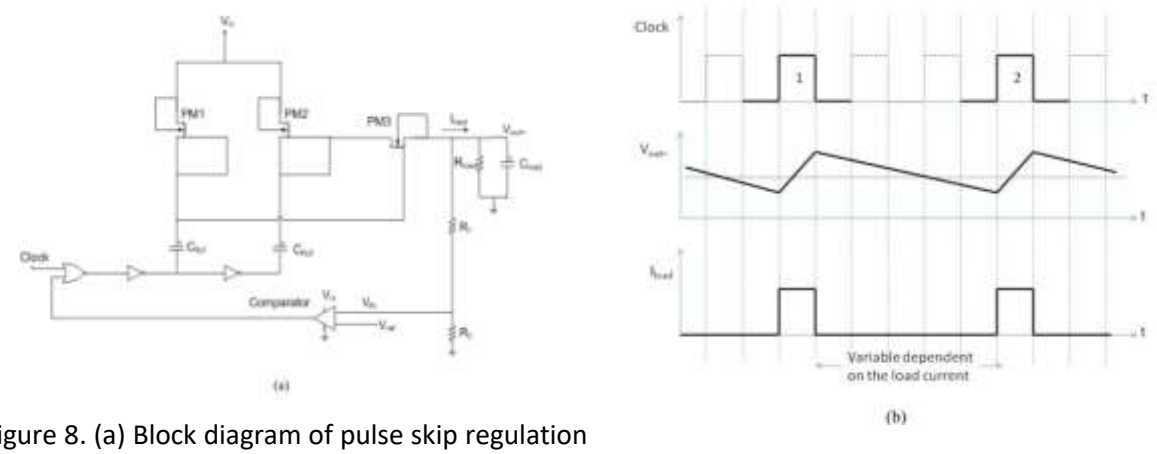

Figure 8. (a) Block diagram of pulse skip regulation method [11] (b) Skipping of the clock signal for high load current requirement [10].

Fixed Frequency Regulation (Pulse Width Modulation Technique)

In the fixed frequency regulation scheme, the duty cycle of the clock signal is modulated to regulate the output voltage. The duty cycle modulation of the clock signal depends either on the input voltage or on the load requirement [12]. The block diagram of pulse width modulation control for charge pump architecture is shown in Fig. 9. If the input voltage increases or the load current goes low, the output voltage of charge pump increases and it is fed back to an error amplifier. The output of the amplifier is compared against a saw tooth waveform using a comparator. For higher output voltage, the duty cycle of the clock signal becomes narrow and the average power delivered to the load during each clock cycle goes down. In case of low output voltage and high loading requirement, the output voltage decreases which causes an increase in the duty cycle of the clock signal. Thus, the average energy delivered to the load during each clock cycle rises as well as the output voltage [12].

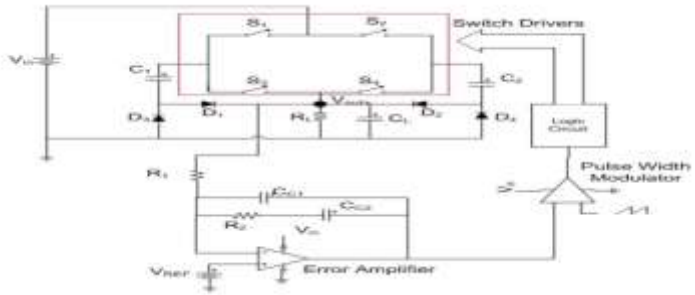

Figure 9. Schematic of buck charge pump with pulse width modulation technique [12]

Linear Skip Regulation Method: The linear skip control method is more complex than the pulse skip regulation method and helps in enhancing the output ripple voltage performance of the charge pump. The linear skip regulation scheme uses three phases of operation, which are wait state, transfer phase, and charge phase [13]. When the load current is high, there is no wait state and the current supplied to the output load is regulated by charge and transfer phases. When the output voltage increases due to either high input voltage or low load current, the wait time increases and the operation of the charge pump stops. During the wait state, the charge delivered

to the load is supplied by the load capacitor. Fig. 10 depicts the switching clock signals for the linear skip regulation method employed in the switched-capacitor DC-DC converter.

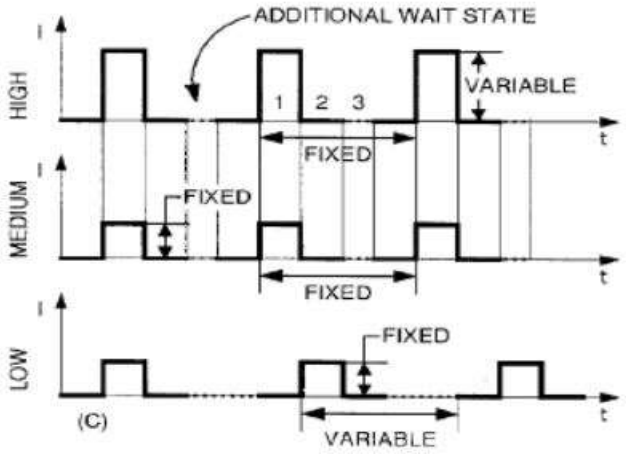

Figure 10. Clock signals for different loading current requirement in linear skip regulation method [13]

In summury , advantages and disadvantages of regulation methods are shown in the following table :

Table 1. Advantages and disadvantages of regulation methods

Regulation method	Advantages	Disadvantages
Pulse Skip Regulation	Very low quiescent current	High output voltage ripple –No fixed frequency
Constant Frequency Regulation	Very low voltage ripple , Fixed frequency	Higher quiescent current
Linear Skip Regulation	Low output voltage ripple , Low quiescent current	For very low output currents no fixed frequency

3.3. Charge pumps modeling

The state behavior of a switched capacitor (SC) converter can be modeled as an ideal transformer with a serial output impedance in the case of neglecting frequency dependant parasitic losses as shown in Fig.11.

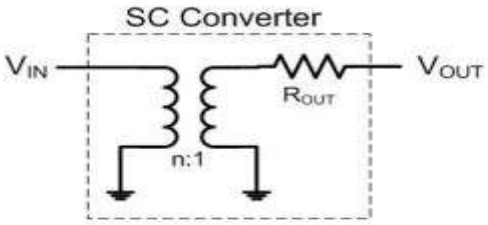

Figure 11. Model of a charge pump converter [14]

Where n represents the conversion ration which is related to converter topology and switching pattern .The requisite output voltage drop used to move charge in the circuit is represented by the output impedance which is a function of converter topology , switching frequency and component sizes.Charge pumps can operate at low switching frequencies , the regime is called slow switching limit (SSL) , converter losses and output impedance are dominated by amount of charge that can be transferred by capacitor. At high frequencies , the regim is called fast switching

limit (FSL) , in this conditions , switch on –state resistance prevents capacitors from completely transferring their charge each period.

If we assume two-phase converters operating at 50% duty cycle. The SSL (capacitor-dominated) and FSL (switch-dominated) output impedance are given by the following equations [15]:

$$R_{SSL} = \frac{1}{f_{SW}} \frac{(a_{c,i})^2}{2C_i} \quad (25)$$

$$R_{FSL} = 2R_i (a_{r,i})^2 \quad (26)$$

Where f_{SW} is the switching frequency, C_i value of capacitor i and $a_{c,i}$ charge multiplier of a capacitor i , R_i represents on-state resistance and $a_{r,i}$ charge multiplier for a switch i.

Expressions of output impedance for a charge pump converter facilitate its optimazation.Each circuit element can be sized proportionally to its charge multiplier and inversely to its blocking voltage by constraining total switch V-A product (related to area for integrated implementations). This optimization yields the smallest output impedance for a given allotment of switch V-A product or capacitor energy storage [14].We can develop a pair of performances metrics from the output impedance expressions , after applying optimization , in order to express ratio of the optimized performance of a charge pump to the cost of components used. In the case of the slow switching limit, the dimensionless metric in is the ratio of the converter output GV^2 to the total energy storage scaled by switching frequency. In the case of the fast switching limit, the metric is the ratio of the converter output GV^2 to the value of the GV^2 ratings of the switches, totaled over the switches. Converter output GV 2 is a precise metric that allows an exact computation of a power versus loss relationship. These metrics assume the switches and capacitors are sized optimally as described above and in [14]. The SSL and FSL metrics are given as follows:

$$M_{SSL} = \frac{2V_{OUT}{}^2}{(i \in caps|a_{c,i}V_{c,i(rated)}|)^2} \quad (27)$$

$$M_{FSL} = \frac{V_{OUT}{}^2}{2(i \in sw|a_{r,i}V_{r,i(rated)}|)^2} \quad (28)$$

These metrics depends only on the squared-absolute-sum of the V-A products for the relevant circuitelements – capacitors or switches – normalized by output power. Thus, the performance metrics relate directly to the fundamental operation of the underlying circuit. In the performance metrics, the voltage used for characterization is the component voltage rating, since this sets the cost of the device [14].

4. Inductor DC/DC converters Vs charge pumps circuits

As industry pushes towards system on chip (SOC) solutions , circuits are integrated onto a single die , and the power converters occupy an increasing proportion of printed circuit board (PCB) area .Inductors are larger compared to ceramic capacitors used in charge pumps architectures . Even though the switching rate in modern systems has increased and the size of inductor used in DC-DC converter has been reduced, the integration of an inductor on the chip is still difficult compared to a capacitor. Moreover, the cost of an inductor is also 5 to10 times higher than a flying capacitor used in the charge pump[2]. In contrast to inductor DC-DC converters , charge pumps require only capacitors, which have a significantly higher power density and can be integrated more easily than inductors. Historically, charge pumps have been used in integrated circuits to provide programmable voltages to memories, and have mostly been limited to low power (<100mW) applications. However, SC converters theoretically have lower

intrinsic conduction loss than inductor-based converters for a given total rating (e.g. V-A product) of switches for certain converters or applications [14].

In brief , main differences between inductor DC-DC converters and charge pumps are given in the following table

Table 2. Charge pumps Vs inductor DC-DC converters

Charge pump characteristics	Inductor DC-DC converter characteristics
High power conversion efficiency over limited input voltage range	High power conversion efficiency over wide input voltage
Low quiescent current	Low quiescent current
High power conversion efficiency over limited input voltage range	High power conversion efficiency over wide input voltage
Small board size of total solution	High transformation ratio
Ease of use	(rather large)inductor
Extremely low EMI ,low output voltage ripple	Low EMI difficult to reach

5. Battery operated system design considerations

5.1. Toplogy selection

The topology selection is the first step of a portable power circuit design. It is mainly based on the input and output voltage rating, as shown in Fig. 18. If the input voltage is higher than the output at any time, a Buck converter or LDO is normally the only solution. If the input voltage is lower than the output voltage, a Boost converter can be employed while a charge pump converter could be used for low current and low cost applications. Both Buck-Boost and Flyback can be used for the case that the battery voltage can be either higher or lower than the output voltage. However, Flyback is normally more suitable for a higher output voltage case [16].

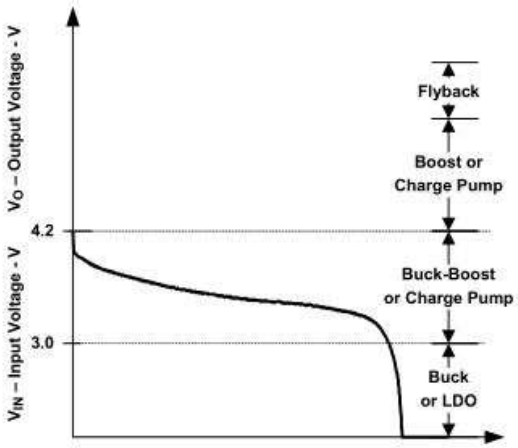

Figure 12. Voltage considerations for topology selection for single-cell Li-ion battery

5.2. Volatge regulation accuracy

Output voltage regulation accuracy is one of the key specifications for any DC-DC converter. The output voltage accuracy mainly depends on internal reference voltage accuracy, feedback voltage accuracy, internal error amplifier DC gain and its offset voltage, feedback resistor divider accuracy, and system voltage loop DC gain. The feedback voltage at the non-inverting input of the voltage error amplifier specifies the possible voltage tolerance associated with the internal band-gap voltage reference through a voltage buffer over the full temperature range. This usually includes the offset voltage of the internal voltage error amplifier. It should be noted that the lower the feedback voltage, the higher the contribution tolerance due to the offset voltage. The closed loop DC gain has a significant impact on the DC regulation accuracy. The higher the DC gain of the voltage loop, the higher the output voltage regulation accuracy. This is why a low-frequency pole such as an integrator is usually placed in the voltage loop compensator. The output voltage error in the closed voltage loop is given by the following equation [16]

$$\frac{\Delta V_{OUT}}{V_{REF}} = \frac{1}{1+G_1G_2G_3} \quad (29)$$

V_{REF} is the reference voltage at the non –inverting error amplifier , G_1 is the DC gain of voltage error amplifier with loop compensator , G_2 PWM comparator gain , G_3 power stage gain from duty cycle to output voltage

6. Conclusion

The demand for portable, thin, lightweight and multifunctional consumer electronic devices (i.e., mobile phones, laptops) is growing day-to-day. Portable devices are powered from single battery and they should be able to operate for an extended period of time. This paper reviews DC-DC converters and charge pump circuits converters .Some topologies of both DC-DC and charge pumps are briefly summarized. The most commonly used regulation schemes for the charge pumps circuits are categorized .Finally, a comparaison between inductor DC-DC converters and charge pumps is established.

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